REMARKS

Claims 1-31 are pending in the subject application. Claims 26-31 have been added by the present amendment. The amendments are fully supported by the specification as originally filed.

As an initial matter, an Information Disclosure Statement (IDS) and Supplemental IDS were filed on April 28, 2003 and May 29, 2003, respectively. The Examiner is requested to return a signed and initialed copy of the Form PTO-1449 indicating that the references listed therein were considered.

The Applicants' claimed invention is directed to a shift register for shifting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, the shift register including: a plurality of flip flops, and a plurality of level shifters for level-shifting (i.e., increasing the voltage of) the clock signal, wherein at least one level shifter is provided for a predetermined number or block of flip flops.

Independent claims 1 and 20 require that when one of the flip flops or a block of flip flop(s) does not require input of the clock signal, the corresponding level shifter is suspended. The level shifter judges a period in which the clock signal must be received by its corresponding flip flop(s), and thus it is possible with the Applicants' invention to control operation of the level shifter based only on the start signal or the output of the previous step (see specification at page 21, second paragraph). According to this arrangement, a distance is reduced between the level shifter and flip flop, thereby simplifying the circuit design and reducing power consumption.

As recited in new claim 26, the level shifter not requiring input of the clock signal is suspended by a reset in accordance with an output of the level shifter of one of the following blocks. Claim 27 requires that each level shifter is reset in accordance with an output of one of the following level shifters.

As shown in FIG. 1, the shift register 11 includes a plurality of flip flops $F1_{(1)}$... and corresponding level shifters $13_{(1)}$... which increase the voltage of a clock signal CK to the flip

flops $F1_{(1)}$... When the flip flop $F1_{(i)}$ does not require input of a clock signal $CK_{(i)}$, operation of the level shifter $13_{(i)}$ is suspended. In such a state, the clock signal $CK_{(i)}$ is not driven, so that there is no power consumption required for driving.

Claims 1-25 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,232,945 to Moriyama et al. (hereinafter "Moriyama") in view of U.S. Patent 6,414,670 to Kim. This rejection is respectfully traversed.

Moriyama fails to teach or suggest a shift register having a plurality of level shifters for level-shifting a clock signal, wherein at least one level shifter is provided for a predetermined number/block of flip flops. As Moriyama fails to provide any disclosure of "a plurality of level shifters" as claimed, it also fails to teach or suggest suspending the level shifter corresponding to a flip flop/block which does not require input of the clock signal.

For example, with reference to FIG. 17 of Moriyama (as cited in the Office Action), a display device and a shift register circuit 21 having a plurality of flip flops 22_1 ... 22_{853} are connected in series, each flip flop transferring a start pulse to the succeeding flip flop in synchronism with a clock pulse (see column 15, lines 11-19). There is no teaching or suggestion of providing a level shifter for each flip flop or block of flip flops, as recited in the Applicants' claimed invention.

The Kim reference fails to remedy the deficiencies of Moriyama. Specifically, Kim fails to teach or suggest providing one level shifter corresponding to each flip flop or block of flip flops.

In FIG. 2 of Kim, as cited in the Office Action, a prior art gate line driver (GD) includes a level changing unit 21, a shift registering unit 22, a level shifting unit 23, and a buffering unit 24 (see column 1, lines 38-41). In particular, the level shifting unit 23 has 154 level shifters "each for shifting a level of a driving signal from the shift registering unit 22" (column 1, lines 47-50).

Therefore, the level shifters disclosed in Kim are provided to level shift the driving signal, not the clock signal as recited in the Applicants' claimed invention.

In Kim, the level changing unit 21 increases the voltage of the clock signal. In contrast, according to the Applicants' claimed invention, the clock signal supplied to the shift register is increased in voltage, and is used to drive the shift register. Therefore, the Applicants' claimed invention is completely different from the arrangement disclosed in the Kim reference.

With reference to the clock generation controlling units 82-1, 82-2, 82-3 ... 82-n as shown in FIG. 8 of Kim and cited in the Office Action, the clock generation controlling units control the application of a clock signal to selective gate line drivers (see column 5, lines 4-20). As shown in FIG. 6 of Kim, the clock generation controlling units are made up two T-flipflops 61a and 61b, an inverter 61c, and two AND gates 61d and 61e (see column 4, lines 17-19). Kim does not teach or suggest "one of the level shifters corresponding to" each flip flop or block of flip flops, as recited in the Applicants' claimed invention. In fact, Kim teaches that the clock generation controlling units each include two flip flops, where the clock generation controlling units 82-1, 82-2, 82-3 ... 82-n are connected to gate-line drivers 81-1, 81-2, 81-3 ... 81-n, respectively, the gate-line drivers having level shifters for level shifting the driving signal (see FIGS. 2 and 8).

Therefore, Kim does not teach or suggest a one-to-one correspondence between a level shifter and flip flop(s), as recited in the Applicants' claimed invention. In the Applicants' claimed invention, each flip flop receives the clock signal that has been increased in voltage by the level shifter of the corresponding block of flip flop(s). As a result, it is possible to shorten the total length of wires connecting the level shifters with the flip flops, thereby decreasing the current value necessary for supplying the clock signal.

In Kim, the clock signal is increased in voltage by the level changing unit alone, and is supplied to each flip flop. Therefore, the total length of wires connecting the level changing unit with each flip flop is long. As a result, the current value necessary for supplying the clock signal

is high. Accordingly, power consumption is increased in Kim, as compared to the Applicants' invention.

While Kim discloses an arrangement in which a supply of the clock signal is shut off, there is no teaching or suggestion for suspending the operation of a level shifter or shift register to reduce power consumption. Therefore, even if Kim were somehow combined with Moriyama, it would not be possible to produce the Applicants' claimed invention.

For the above reasons, the claims should now be in condition for immediate allowance. However, if there are any outstanding issues, the Examiner is urged to call the undersigned at the phone number listed below.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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